CLAIMS

1. A circuit providing protection against electrostatic discharge (ESD) for internal elements of an Integrated Circuit (IC), the circuit being connected to a power rail and a ground rail and to an inverter of a clamp preamplifier, said circuit is characterized in that it comprises:

- a PMOSFET resistor (R) with a gate connected to said ground rail (VSS), a drain connected to said inverter's (INV) input node (ESD_RC), a source and a bulk connected to said power rail (VDD),
- an NMOSFET capacitor (C1) with a gate connected to said inverter's (INV) input node (ESD_RC), a drain, a source and a bulk connected to said ground rail (VSS), and
- a PMOSFET capacitor (C2) with a gate connected to said inverter's (INV) input node (ESD_RC), a drain, a source connected to said ground rail (VSS) and a bulk connected to said power rail (VDD).

2. The circuit according to claim 1 wherein said NMOSFET capacitor (C1) has a non-linear characteristic.

3. The circuit according to claim 1 wherein said PMOSFET capacitor (C2) has a non-linear characteristic.

4. The circuit according to claim 1 wherein said NMOSFET capacitor (C1) and said PMOSFET capacitor (C2) have non-linear characteristics.

5. The circuit according to any of the claims 1-4 wherein ratio of capacitance of said PMOSFET capacitor (C2) to capacitance of said NMOSFET capacitor (C1) decreases when voltage at said power rail (VDD) exceeds NMOSFET threshold.

6. An integrated circuit comprising a circuit

providing protection against an electrostatic discharge event according to any of claims 1-5.